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EXAMINER	
PAREKH, NITIN	
ART UNIT	**PAPER NUMBER**
2811	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/420,086	Applicant(s) FARNWORTH ET AL.	
	Examiner Nitin Parekh	Art Unit 2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 August 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *25-39 and 47-53* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *25-39 and 47-53* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 October 1999* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)
2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3)☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4)☐ Interview Summary (PTO-413) Paper No(s). _____ .
5)☐ Notice of Informal Patent Application (PTO-152)
6)☐ Other: .

DETAILED ACTION

Request for Continued Examination

1. A request for continued examination (RCE) under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 08/12/03 and 08/15/03 have been entered. An action on the RCE follows.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 25, 26, 28-33, 35-37, 39, 47, 48 and 51-53 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chou et al. (US Pat. 5691568).

Regarding claim 25, Chou et al. disclose a semiconductor component/assembly/package (1000 in Fig. 10A/10B; Col. 16, lines 5-21) comprising:

- a substrate made of material such as a printed circuit board (PCB), plastic/epoxy laminate, ceramic, etc. (not numerically referenced in Fig. 10A/10B- Col. 1, line 53; Col. 10, line 29; Col. 16, line 46) having top and bottom surfaces
- a conductive layer (512/1011a-1011d in Fig. 10A/10B) having land segments comprising a plurality of first portions (1011a and 1011d in Fig. 10A/10B) and a plurality of second portions (1011b, 1011c and 512 in Fig. 10A/10B)
- a plurality of conductors on the first and second portions comprising conductive pads/sites (not numerically referenced- see bonding pads/sites on 1011a, 1011b, etc. connected by bonding wires in Fig. 10A), those on the first portions being separated and electrically isolated from one another by those on the second portions of the conductive layer (see 1011a/1011d being spaced from 1011b in Fig. 10A/10B)
- a plurality of recesses/grooves (not numerically referenced- see recesses/grooves having predetermined size, shape and width in Fig. 10A/10B between the conductive portions of the conductive layer) in the conductive layer defining a size, a spacing and a shape (Col. 11, lines 20-24) of the conductors and the second portions of the conductive layer
- a semiconductor die (die 502 in Fig. 10A/10B) on the top surface of the substrate in an electrical communication with the conductors comprising conductive portions/conductive pads

- a plurality of electrically conductive vias through the substrate (1034a, 1034b, etc. in Fig. 10A/10B) in electrical communication with the conductors/conductive pads (1011a, 1011b, etc. respectively in Fig. 10A) and
- a plurality of external contacts/balls (not numerically referenced in Fig. 10A- see 522a-522e in Fig. 5B; Col.16, lines 46-53) in a ball grid array (BGA) on the bottom surface of the substrate, the external contacts/balls being in electrical communication with the respective conductive vias and conductive portions of the conductive layer (Col. 16, lines 33-38)

(Fig. 10A/10B; Fig. 5A-5G; Col. 16, line 5- Col. 17, line 15).

Chou et al. fail to teach the plurality of first and second portions of the conductive layer substantially covering the surface of the substrate.

Chou et al. further teach in another embodiment (Fig. 11A/11B), the conductive layer being extended to include a thermally and an electrically conductive die attach/paddle metal area (Col. 17, lines 16-50), the die attach/paddle metal area being selectively connected with one or more of the land segment/pad region of the first or second portions of the conductive layer to provide a significant increase in the area covering the surface of the substrate and to provide the enhanced thermal dissipation and heat transfer from the die (Col. 17, lines 50-65).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the plurality of first and second portions of the conductive layer substantially covering the surface of the substrate as taught by Chou et al. in the embodiment of Fig. 11A/11B so that the thermal dissipation and electrical performance/grounding can be improved in Chou et al's component.

Regarding claim 26, Chou et al. teach substantially the entire claimed structure as applied to claim 25, wherein Chou et al. teach the semiconductor die being wire bonded to the respective plurality of conductive pads/sites on the conductors (see wire bonds 1026a, 1026b, etc. in Fig. 10A).

Regarding claim 28, Chou et al. teach substantially the entire claimed structure as applied to claim 25, wherein Chou et al. teach the substrate (not numerically referenced in Fig. 10A/10B; Col. 10, line 29; see 504 in Fig. 5A) comprising a material including plastic or ceramic (Col. 1, line 53;; Col. 16, line 46).

Regarding claim 29, Chou et al. teach substantially the entire claimed structure as applied to claim 25, wherein Chou et al. teach the conductors comprising the plurality of external contacts/balls (not numerically referenced in Fig. 10A- see 522a, 522b, etc. in Fig. 5B; Col. 10, lines 35-40; Col.16, lines 46-53) being adapted/adaptable for the electrical connection to the external/outside circuitry.

Regarding claim 30, Chou et al. disclose a semiconductor component/assembly/package (1000 in Fig. 10A/10B; Col. 16, lines 5-21) comprising:

- a substrate made of material such as a printed circuit board (PCB), plastic/epoxy laminate, ceramic, etc. (not numerically referenced in Fig. 10A/10B- Col. 1, line 53; Col. 10, line 29; Col. 16, line 46) having top and bottom surfaces
- a conductive layer (512/1011a-1011d in Fig. 10A/10B) having land segments comprising a plurality of conductors (1011a, 1011b, 1011c, etc. Fig. 10A/10B),

the conductive layer comprising a metal layer/foil (Col. 10, lines 35-38) being attached/disposed on the top surface of the substrate

- the plurality of conductors having respective conductive pads/sites (see bonding pads/sites on 1011a, 1011b, etc. connected by bonding wires in Fig. 10A) for electrical connections
- a plurality of recesses/grooves (not numerically referenced- see recesses/grooves between the conductors in Fig. 10A/10B) in the metal layer/foil defining a size, a spacing and a shape (Col. 11, lines 20-24) of the conductors, each conductor being defined by a groove/recess having a portion of the metal layer/foil on either side (see 1011b being separated by the groove/recess and having 1011a and 1011d on both sides in Fig. 10A/10B)
- a semiconductor die (die 502 in Fig. 10A/10B) being wire bonded to the top surface of the substrate in an electrical communication with the conductors/conductive pads
- a plurality of electrically conductive vias through the substrate (1034a, 1034b, etc. in Fig. 10A/10B) in electrical communication with the conductors (1011a, 1011b, etc. respectively in Fig. 10A) and
- a plurality of external contacts/balls (not numerically referenced in Fig. 10A- see 522a-522e in Fig. 5B; Col.16, lines 46-53) in a ball grid array (BGA) on the bottom surface of the substrate, the external contacts/balls being in electrical communication with the respective conductive vias and conductive portions of the conductive layer (Col. 16, lines 33-38)

(Fig. 10A/10B; Fig. 5A-5G; Col. 16, line 5- Col. 17, line 15).

Chou et al. fail to teach the conductive layer substantially covering the surface of the substrate.

Chou et al. further teach in another embodiment (Fig. 11A/11B), the conductive layer being extended to include a thermally and an electrically conductive die attach/paddle metal area (Col. 17, lines 16-50), the die attach/paddle metal area being selectively connected with one or more of the land segment/pad region of the conductive layer to provide a significant increase in the area covering the surface of the substrate and to provide the enhanced thermal dissipation and heat transfer from the die (Col. 17, lines 50-65).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the conductive layer substantially covering the surface of the substrate as taught by Chou et al. in the embodiment of Fig. 11A/11B so that the thermal dissipation and electrical performance/grounding can be improved in Chou et al's component.

Regarding claim 31, Chou et al. teach substantially the entire claimed structure as applied to claim 30, wherein Chou et al. teach the conductors comprising the plurality of external contacts/balls (not numerically referenced in Fig. 10A- see 522a, 522b, etc. in Fig. 5B; Col. 10, lines 35-40; Col.16, lines 46-53) being adapted/adaptable for the electrical connection to the external/outside circuitry.

Regarding claim 32, Chou et al. teach substantially the entire claimed structure as applied to claim 30, wherein Chou et al. teach the plurality of conductive vias through the substrate (1034a, 1034b, etc. in Fig. 10A/10B) in electrical communication with the respective conductors (1011a, 1011b, etc. respectively in Fig. 10A) and the plurality of external contacts/contact balls (not numerically referenced in Fig. 10A- see 522 a-522e in Fig. 5B; Col.16, lines 46-53) on the bottom/second surface of the substrate.

Regarding claim 33, Chou et al. teach substantially the entire claimed structure as applied to claim 30, wherein Chou et al. teach the component comprising the assembly/package (1000 in Fig. 10A/10B; Col. 16, line 39).

Regarding claim 35, Chou et al. disclose a semiconductor component/assembly/package (1000 in Fig. 10A/10B; Col. 16, lines 5-21) comprising:

- a substrate made of material such as a printed circuit board (PCB), plastic/epoxy laminate, ceramic, etc. (not numerically referenced in Fig. 10A/10B- Col. 1, line 53; Col. 10, line 29; Col. 16, line 46) having top and bottom surfaces
- a conductive layer (512/1011a-1011d in Fig. 10A/10B) having land segments comprising a plurality of first portions (1011a and 1011d in Fig. 10A/10B) and a plurality of second portions (1011b and 1011c in Fig. 10A/10B)
- a plurality of conductors comprising conductive pads/sites (not numerically referenced- see bonding pads/sites on 1011a, 1011b, etc. connected by bonding wires in Fig. 10A) on the first portions of the conductive layer being separated and electrically isolated from one another by the second portions of the

conductive layer (see 1011a/1011d being spaced from 1011b by a recess/groove in Fig. 10A/10B)

- a plurality of recesses/grooves (not numerically referenced- see recesses/grooves in Fig. 10A/10B) in the conductive layer defining a size, a spacing, a shape and side edges of the conductors (see vertical edges of 1011a, 1011b, etc. in Fig. 10A; Col. 11, lines 20-24),
- each conductor being defined by a pair of grooves/recesses and being separated from the adjacent conductor portions, each adjacent first portions of the conductive layer being separated by the second portions of the conductor (see 1011d and 1011 having the edges defined by the grooves/recesses
- a semiconductor die (die 502 in Fig. 10A/10B) being wire bonded to the top surface of the substrate in an electrical communication with the conductors comprising conductive portions
- a plurality of electrically conductive vias through the substrate (1034a, 1034b, etc. in Fig. 10A/10B) in electrical communication with the conductors (1011a, 1011b, etc. respectively in Fig. 10A), and
- a plurality of external contacts/balls (not numerically referenced in Fig. 10A- see 522a-522e in Fig. 5B; Col.16, lines 46-53) in a ball grid array (BGA) on the bottom surface of the substrate, the external contacts/balls being in electrical communication with the respective conductive vias and conductive portions of the conductive layer (Col. 16, lines 33-38)

(Fig. 10A/10B; Fig. 5A-5G; Col. 16, line 5- Col. 17, line 15).

Chou et al. fail to teach the conductive layer substantially covering the surface of the substrate.

Chou et al. further teach in another embodiment (Fig. 11A/11B), the conductive layer being extended to include a thermally and an electrically conductive die attach/paddle metal area (Col. 17, lines 16-50), the die attach/paddle metal area being selectively connected with one or more of the land segment/pad region of the first or second portions of the conductive layer to provide a significant increase in the area covering the surface of the substrate and to provide the enhanced thermal dissipation and heat transfer from the die (Col. 17, lines 50-65).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the conductive layer substantially covering the surface of the substrate as taught by Chou et al. in the embodiment of Fig. 11A/11B so that the thermal dissipation and electrical performance/grounding can be improved in Chou et al's component.

Regarding claim 36, Chou et al. teach substantially the entire claimed structure as applied to claim 35, wherein Chou et al. teach the semiconductor die being wire bonded to the respective plurality of conductive pads/sites on the conductive portions (see wire bonds 1026a, 1026b, etc. in Fig. 10A).

Regarding claim 37, Chou et al. teach substantially the entire claimed structure as applied to claim 35, wherein Chou et al. teach the plurality of conductive pads/sites being wire bonded to the die (see wire bonds 1026a, 1026b, etc. bonding the conductors to respective pads on the die in Fig. 10A) and the plurality of external

contacts/balls (not numerically referenced in Fig. 10A- see 522a, 522b, etc. in Fig. 5B; Col. 10, lines 35-40;
Col.16, lines 46-53) being adapted/adaptable for the electrical connection to the external/outside circuitry.

Regarding claim 39, Chou et al. teach substantially the entire claimed structure as applied to claim 35, wherein Chou et al. teach the substrate (not numerically referenced in Fig. 10A/10B) comprising the material including plastic or ceramic (Col. 1, line 53; Col. 10, line 29; Col. 16, line 46).

Regarding claim 47, Chou et al. disclose a semiconductor component/assembly/package (1000 in Fig. 10A/10B; Col. 16, lines 5-21) comprising:

- a substrate made of material such as a printed circuit board (PCB), plastic/epoxy laminate, ceramic, etc. (not numerically referenced in Fig. 10A/10B- Col. 1, line 53; Col. 10, line 29; Col. 16, line 46) having top and bottom surfaces
- a conductive layer (512/1011a-1011d in Fig. 10A/10B) comprising a plurality of portions (1011a, 1011b, 1011c, etc. in Fig. 10A/10B), the conductive portions having a plurality of respective conductors comprising conductive pads/sites (see bonding pads/sites on 1011a, 1011b, etc. connected by bonding wires in Fig. 10A) for electrical connections
- a plurality of recesses/grooves (not numerically referenced- see recesses/grooves in Fig. 10A/10B) in the conductive layer defining a size, a spacing and a shape (Col. 11, lines 20-24) of the conductors, each conductor having opposing edges (see vertical edges of 1011a-1011d in Fig. 10A) being

defined by a pair of grooves/recesses (see the pair of grooves/recesses on both sides of 1011a-1011d in Fig. 10A) and each conductor having the portions of the conductive layer on either side being separated from the opposing edges by the pair of grooves/recesses

- a semiconductor die (die 502 in Fig. 10A/10B) being wire bonded on the top surface of the substrate in an electrical communication with the conductors/conductive pads
- a plurality of electrically conductive vias through the substrate (1034a, 1034b, etc. in Fig. 10A/10B) in electrical communication with the conductors (1011a, 1011b, etc. respectively in Fig. 10A) and
- a plurality of external contacts/balls (not numerically referenced in Fig. 10A- see 522a-522e in Fig. 5B; Col.16, lines 46-53) in a ball grid array (BGA) on the bottom surface of the substrate, the external contacts/balls being in electrical communication with the respective conductive vias and conductive portions of the conductive layer (Col. 16, lines 33-38)

(Fig. 10A/10B; Fig. 5A-5G; Col. 16, line 5- Col. 17, line 15).

Chou et al. fail to teach the conductive layer substantially covering the surface of the substrate.

Chou et al. further teach in another embodiment (Fig. 11A/11B), the conductive layer being extended to include a thermally and an electrically conductive die attach/paddle metal area (Col. 17, lines 16-50), the die attach/paddle metal area being selectively connected with one or more of the land segment/pad portion of the

conductive layer to provide a significant increase in the area covering the surface of the substrate and to provide the enhanced thermal dissipation and heat transfer from the die (Col. 17, lines 50-65).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the conductive layer substantially covering the surface of the substrate as taught by Chou et al. in the embodiment of Fig. 11A/11B so that the thermal dissipation and electrical performance/grounding can be improved in Chou et al's component.

Regarding claim 48, Chou et al. teach substantially the entire claimed structure as applied to claim 47, wherein Chou et al. teach the semiconductor die being wire bonded to the respective plurality of conductive pads on the conductive portions (see wire bonds 1026a, 1026b, etc. in Fig. 10A).

Regarding claim 51, Chou et al. teach substantially the entire claimed structure as applied to claim 47 above, wherein Chou et al. teach the conductive layer (512/1011a-1011d in Fig. 10A/10B) having an opening in a central portion for attaching/bonding the die to the substrate (see Fig. 10A).

Regarding claim 52, Chou et al. disclose a semiconductor component/assembly/package (1000 in Fig. 10A/10B; Col. 16, lines 5-21) comprising:

- a substrate made of material such as a printed circuit board (PCB), plastic/epoxy laminate, ceramic, etc. (not numerically referenced in Fig. 10A/10B- Col. 1, line 53; Col. 10, line 29; Col. 16, line 46) having top and bottom surfaces
- a conductive layer (512/1011a-1011d in Fig. 10A/10B) having land segments comprising a plurality of conductive portions including first portions (1011a and 1011d in Fig. 10A/10B) and second portions (1011b and 1011c in Fig. 10A/10B),
- a plurality of conductors comprising first and second portions including conductive pads/sites (not numerically referenced- see bonding pads/sites on 1011a/1011d and 1011b/1011c respectively connected by bonding wires in Fig. 10A)
- the plurality of conductors having a size, a spacing and a shape defined by a plurality of recesses/grooves (not numerically referenced- see recesses/grooves in Fig. 10A/10B) through the conductive layer, each first portion of the conductor being separated from an adjacent conductor by the groove/recess and the second portion of the conductor (see 1011a and 1011d being spaced from 1011b by a recess/groove in Fig. 10A/10B)
- a semiconductor die (die 502 in Fig. 10A/10B) being wire bonded on the top surface of the substrate in an electrical communication with the conductors comprising conductive portions/conductive pads
- a plurality of electrically conductive vias through the substrate (1034a, 1034b, etc. in Fig. 10A/10B) in electrical communication with the conductors (1011a, 1011b, etc. respectively in Fig. 10A), and

- a plurality of external contacts/balls (not numerically referenced in Fig. 10A- see 522 a-522e in Fig. 5B; Col.16, lines 46-53) in a ball grid array (BGA) on the bottom surface of the substrate, the external contacts/balls being in electrical communication with the respective conductive vias and conductive portions of the conductive layer (Col. 16, lines 33-38)

(Fig. 10A/10B; Fig. 5A-5G; Col. 16, line 5- Col. 17, line 15).

Chou et al. fail to teach the conductive layer substantially covering the surface of the substrate.

Chou et al. further teach in another embodiment (Fig. 11A/11B), the conductive layer being extended to include a thermally and an electrically conductive die attach/paddle metal area (Col. 17, lines 16-50), the die attach/paddle metal area being selectively connected with one or more of the land segment/pad regions of the first or second portions of the conductive layer to provide a significant increase in the area covering the surface of the substrate and to provide the enhanced thermal dissipation and heat transfer from the die (Col. 17, lines 50-65).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the conductive layer substantially covering the surface of the substrate as taught by Chou et al. in the embodiment of Fig. 11A/11B so that the thermal dissipation and electrical performance/grounding can be improved in Chou et al's component.

Regarding claim 53, Chou et al. teach substantially the entire claimed structure as applied to claim 25, wherein Chou et al. teach the plurality of external contacts/balls (not numerically referenced in Fig. 10A- see 522a, 522b, etc. in Fig. 5B; Col. 10, lines 35-40; Col.16, lines 46-53) on the substrate in electrical connection with the conductive vias (1036a-1036d in Fig. 10B; Col. 16, lines 33-38).

4. Claims 27 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chou et al. (US Pat. 5691568) in view of Pedder (US Pat. 5717245).

Regarding claim 27, Chou et al. teach substantially the entire claimed structure as applied to claim 25, except the die being flipchip mounted to the conductors.

Pedder teaches a BGA package having multichip module (MCM) where chips are electrically connected to conductive portions of the substrate using conventional configurations including a wire bonding connection (43 in Fig. 2) and flipchip mounting connections (41/42 in Fig. 2; Col. 4, lines 43-49).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the die being flipchip mounted to the conductors as taught by Pedder so that the dimensions of the conductive pads can be reduced and the chip density and electrical performance can be can be improved in Chou et al's component.

Regarding claim 34, Chou et al. teach substantially the entire claimed structure as applied to claim 30, except an encapsulant at least partially covering the die and a portion of the surface.

Pedder teaches using a sealant/encapsulant to encapsulate the BGA package/module (Col. 1, line 55).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the encapsulant covering the die and a portion of the surface as taught by Pedder so that the surface protection for the electrical connections can be improved and the damage from contamination and moisture can be reduced in Chou et al's component.

5. Claim 38 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chou et al. (US Pat. 5691568) in view of Beaman et al. (US Pat. 5531022).

Regarding claim 38, Chou et al. teach substantially the entire claimed structure as applied to claim 35, wherein Chou et al. further teach the substrate comprising an insulating layer on the surface (not numerically referenced in Fig. 10A- see 506a in Fig. 5A-5C; Col. 10, line 23; Col. 16, line 21), but Chou et al. fail to teach the substrate comprising a semiconductor material.

Beaman et al. teach using a high performance package (2 in Fig. 1) having a multilayered substrate (MLS) where the substrate (8 in Fig. 1) comprises an insulating layer and a semiconductor material such as silicon (Col. 3, line 48) to improve thermal conductivity (Col. 3, lines 45-52).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the substrate comprising the semiconductor material as taught by Beaman et al. so that the thermal dissipation and electrical performance can be improved in Chou et al's component.

6. Claims 49 and 50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chou et al. (US Pat. 5691568) in view of Rostoker et al. (US Pat. 6181011).

Regarding claims 49 and 50, Chou et al. teach substantially the entire claimed structure as applied to claim 47 above, wherein Chou et al. further teach using a reduced pitch between the lands/pads and using shorter bonding wires to provide reduced impedance and improved manufacturing yield and reliability (Col. 16, lines 55-67), but Chou et al. fail to teach each conductor or each groove having a first width and a second width of about 5 microns respectively.

Rostoker et al. teach using a semiconductor component in a variety of packages including a BGA package where wiring/conductor dimensions such as width (W), spacing/groove size (S), thickness (T), etc. (Fig. 4; Col. 9, lines 15-20) are optimized in order to reduce the capacitance and interconnect delay and to improve the speed and package performance (Col. 9, line 15- Col. 10, line 30). Furthermore, the width (W) and space/groove (S) dimensions have a range of values including a range of 0.16-20 microns for the width dimension and a ratio W/S being in a range of 0.7-1.0 (Col. 10, lines 5-20; see W and W/S values and ratios listed in Table in Col. 10).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate each conductor or each groove having a first width and a second width of about 5 microns as taught by Rostoker et al. so that the capacitance and interconnect delay can be reduced and the speed/performance of the package can be improved in Chou et al's component.

Response to Arguments

7. Applicant's arguments with respect to claims 25-39 and 47-53 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. References C and D are cited as being related to chip component having conductive planes and wiring patterns.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number is 703-305-3410. The examiner can normally be reached on 09:00AM-05:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 703-308-1690. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-306-3431.

Nitin Parekh

NP

10-28-03

NITIN PAREKH

PATENT EXAMINER